UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/654,893	09/05/2003	Kiyoshi Hayase	242358US2	6644

22850	7590	11/09/2006

C. IRVIN MCCLELLAND
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
SCHELL, JOSEPH O

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/654,893	HAYASE, KIYOSHI
	Examiner	Art Unit	
	Joseph Schell	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *15 August 2006*.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *2-6* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *2-6* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1. ☐ Certified copies of the priority documents have been received.

   2. ☐ Certified copies of the priority documents have been received in Application No. _____.

   3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Detailed Action

Claims 2-6 have been examined.

Claims 2-6 have been rejected.

Response to Arguments

1.   Applicant's arguments filed August 15, 2006 have been fully considered but they
are not persuasive. Regarding newly independent claims 2-4, Applicant argues that
Debling ('592) does not teach a selecting circuit for selecting, from among said plurality
of processors, part or all of said plurality of processors to be debugged. The previous
rejection erroneously cited a USB hub as such a selecting circuit and Applicant has
argued that a USB hub simply conveys USB signals without performing any routing
operations on the data flowing therethrough.

The examiner concedes that a USB hub generally only provides a connection as
argued by the Applicant. In the system taught by Debling ('592) there are multiple
processors, each with an on-chip emulator and connected through a USB hub to a
common USB port (as shown in Figure 2). A host controls the debugging through the
USB port (column 4 lines 5-8). Debling ('592) describes the use of a host proxy server
to perform USB functions on behalf of the host (column 4 lines 48-54). In order to target
a specific processor (column 4 lines 5-8) the host proxy server must add USB address
information to a debug command, in addition other USB protocols. The USB device
address embedded in the USB signal allows the host proxy server to select which
specific USB device (since the hub broadcasts downstream signals to all devices) will

execute a command. Also see the attached excerpts from the USB 2.0 Specification for

additional information regarding device addressing.

Claim Objections

2.   Claim 6 line 3 uses the term "from outside." This should be changed to "from an

external device" or "external source".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 2, 3 and 6 are rejected under 35 U.S.C. 103(a) as being obvious over

Debling ('592).

4.   As per claim 2, Debling ('592) discloses a multiprocessor system comprising:

a plurality of processors (column 3 lines 59-63);

at least one debug executing unit for executing the debugging of said plurality of

processors (column 3 lines 59-63, the on-chip emulator);

at least one controller for controlling said debug executing unit (column 3 lines

63-65, the USB interface controller);

a terminal to be connected to an external debugging device (column 4 lines 5-8,

the host contains a connection terminal for sending debug commands);

a selecting circuit for selecting, from among said plurality of processors, part or

all of said plurality of processor to be debugged (column 4 lines 5-8 and 48-54, the

proxy server selects which processor is targeted by a debug command);

said plurality of processors comprise first and second processors (as shown in

figure 2, elements 110),

said debug executing unit comprises a first debug executing unit connected to

said first processor and a second debug executing unit connected to said second

processor (as shown in figure 2, each processor (110) has an on-chip emulator (120)),

said controller comprises a first controller connected to said first debug executing

unit and a second controller connected to second debug executing unit (as shown in

figure 2, each emulator (120) has a USB interface controller (140));

said selecting circuit is connected between said first and second controllers and

said terminal (column 4 lines 48-50, the proxy server exists between the host and the

USB interface of each target processor)

said selecting circuit inputs, to one or both of said first and second controllers, a

debugging signal that is provided from said debugging device through said terminal

(column 4 lines 50-54).

Although in the previous embodiment (as depicted by figure 1) both USB and JTAG

ports are included for debugging, Debling ('592) does not explicitly disclose the

multiprocessor system including a set of terminals for connecting to an external

debugging device. Within the second embodiment, Debling ('592) states that JTAG

circuitry as shown in the first figure may also be provided but it has been omitted for

clarity (column 4 lines 1-2).

At the time of invention it would have been obvious to a person of ordinary skill in the art

to include additional circuitry and ports for JTAG debugging of the processors. This

would have been obvious because a JTAG port would allow the daisy-chaining of other

devices for simultaneous debugging (column 4 lines 29-33).

5.   As per claim 3, Debling ('592) discloses a multiprocessor system comprising:

        a plurality of processors (column 3 lines 59-63);

        at least one debug executing unit for executing the debugging of said plurality of

processors (column 3 lines 59-63, the on-chip emulator);

        at least one controller for controlling said debug executing unit (column 3 lines

63-65, the USB interface controller);

        a terminal to be connected to an external debugging device (column 4 lines 5-8,

the host contains a connection terminal for sending debug commands);

        a selecting circuit for selecting, from among said plurality of processors, part or

all of said plurality of processor to be debugged (column 4 lines 5-8 and 48-54, the

proxy server selects which processor is targeted by a debug command);

said plurality of processors comprise first and second processors (as shown in figure 2, elements 110),

said debug executing unit comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor (as shown in figure 2, each processor (110) has an on-chip emulator (120)),

said selecting circuit is connected between said first and second controllers and said terminal (column 4 lines 48-50, the proxy server exists between the host and the USB interface of each target processor)

said controller is connected to said terminal (column 4 lines 5-9, the remote host communicates through the terminal, this requires a functional connection); and

said selecting circuit inputs, to one or both of said first and second controllers, a debugging signal that is provided from said debugging device through said terminal (column 4 lines 50-54).

Although in the previous embodiment (as depicted by figure 1) both USB and JTAG ports are included for debugging, Debling ('592) does not explicitly disclose the multiprocessor system including a set of terminals for connecting to an external debugging device. Within the second embodiment, Debling ('592) states that JTAG circuitry as shown in the first figure may also be provided but it has been omitted for clarity (column 4 lines 1-2).

At the time of invention it would have been obvious to a person of ordinary skill in the art to include additional circuitry and ports for JTAG debugging of the processors. This would have been obvious because a JTAG port would allow the daisy-chaining of other devices for simultaneous debugging (column 4 lines 29-33).

6.   As per claim 6, Debling ('592) discloses the multiprocessor system according to claim 2, wherein said selecting circuit selects said part or all of said plurality of processors to be debugged, on the basis of a select signal inputted to a given terminal from the outside (column 4 lines 5-8 and 48-54, the host computer creates the debug command which is forwarded to the proxy server (the selector) which converts it to a specific-processor-addressed USB signal).

7.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Debling ('592) in view of Miura (US Patent 6,918,058).

Debling ('592) discloses a multiprocessor system comprising:

          a plurality of processors (column 3 lines 59-63);

          at least one debug executing unit for executing the debugging of said plurality of processors (column 3 lines 59-63, the on-chip emulator);

          at least one controller for controlling said debug executing unit (column 3 lines 63-65, the USB interface controller);

a terminal to be connected to an external debugging device (column 4 lines 5-8, the host contains a connection terminal for sending debug commands);

a selecting circuit for selecting, from among said plurality of processors, part or all of said plurality of processor to be debugged (column 4 lines 5-8 and 48-54, the proxy server selects which processor is targeted by a debug command), wherein

said plurality of processors comprise first and second processors (as shown in figure 2, elements 110),

said debug executing unit is connected to said controller (column 4 lines 5-8, the host forwards debug commands to the on-chip emulators), and

said controller is connected to said terminal (column 4 lines 5-9, the remote host communicates through the terminal, this requires a functional connection).

Although in the previous embodiment (as depicted by figure 1) both USB and JTAG ports are included for debugging, Debling ('592) does not explicitly disclose the multiprocessor system including a set of terminals for connecting to an external debugging device. Within the second embodiment, Debling ('592) states that JTAG circuitry as shown in the first figure may also be provided but it has been omitted for clarity (column 4 lines 1-2).

At the time of invention it would have been obvious to a person of ordinary skill in the art to include additional circuitry and ports for JTAG debugging of the processors. This

would have been obvious because a JTAG port would allow the daisy-chaining of other devices for simultaneous debugging (column 4 lines 29-33).

Debling ('592) does not explicitly disclose the system wherein said selecting circuit inputs, to one or both of said first and second processors, a debugging signal outputted from said debug executing unit. In the multiprocessor system disclosed by Debling ('592), each processor has its own on-chip emulator (as shown by figure 2) with no further processor-selection required below the on-chip emulator level.

Miura ('058) teaches a system that uses a single debugging module to allow an external debugging tool to debug two processors (as shown by figure 1 with the Debugging Tool (3) connected to the single Debugging Module (13) which is connected to first and second microprocessors (elements 10 and 12)).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the debugging system disclosed by Debling ('592) wherein each processor has an associated on-chip emulator, such that a single debugging unit is used for all the processors. This modification would have been obvious because it would avoid unnecessary enlargement of the system and the increased manufacturing costs thereof.

8.   Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Debling ('592) in view of Windows 2000 Device Driver Book.

Debling ('592) discloses the multiprocessor system according to claim 2. Debling ('592) does not explicitly disclose the system wherein said selecting circuit selects said part or all of said plurality of processors to be debugged on the basis of setting of a given register.

Windows 2000 Device Driver Book teaches general information about using device registers for peripheral control.

At the time of invention it would have been obvious to a person of ordinary skill in the art to implement register control within the system disclosed by Debling ('592). This modification would have been obvious because device drivers communicate with a peripheral by reading and writing registers associated with the device (Windows 2000 Device Driver Book chapter 2, section on Device Registers).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Joseph Schell whose telephone number is (571) 272-

8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER